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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,643	07/24/2003	Shinichiro Fujita	116668	9724

25944	7590	05/22/2006

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EXAMINER
BRADLEY, MATTHEW A

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9,13 and 14* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/21/06*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action has been issued in response to amendment filed 21 February 2006. Applicant's arguments have been carefully and fully considered in light of the instant amendment but are not persuasive. Accordingly, this action has been made FINAL.

Claim Status

Claims 8 and 10-12 have been cancelled.

Claims 1-7, 9, and 13-14 remain pending and are ready for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 21 February 2006 was filed on the mailing date for application 10/625,643. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner is considering the information disclosure statement with a signed and initialed copy being attached hereto.

Drawings

The objections to the drawings set forth in the Office action dated 21 November 2005 are withdrawn in light of the drawings filed 21 February 2006.

Specification

The objections to the specification set forth in the Office action dated 21 November 2006 are withdrawn in light of amendments to the specification filed 21 February 2006.

The Examiner objected to the specification with respect to page 4, line 27 having an apparent closed parenthesis mark with no opening parenthesis mark. The Examiner apologizes for this specific objection, but would like to draw the applicant's attention to page 5, line 27, where there is an apparent closed parenthesis mark with no opening parenthesis mark. The specification is hereby objected to.
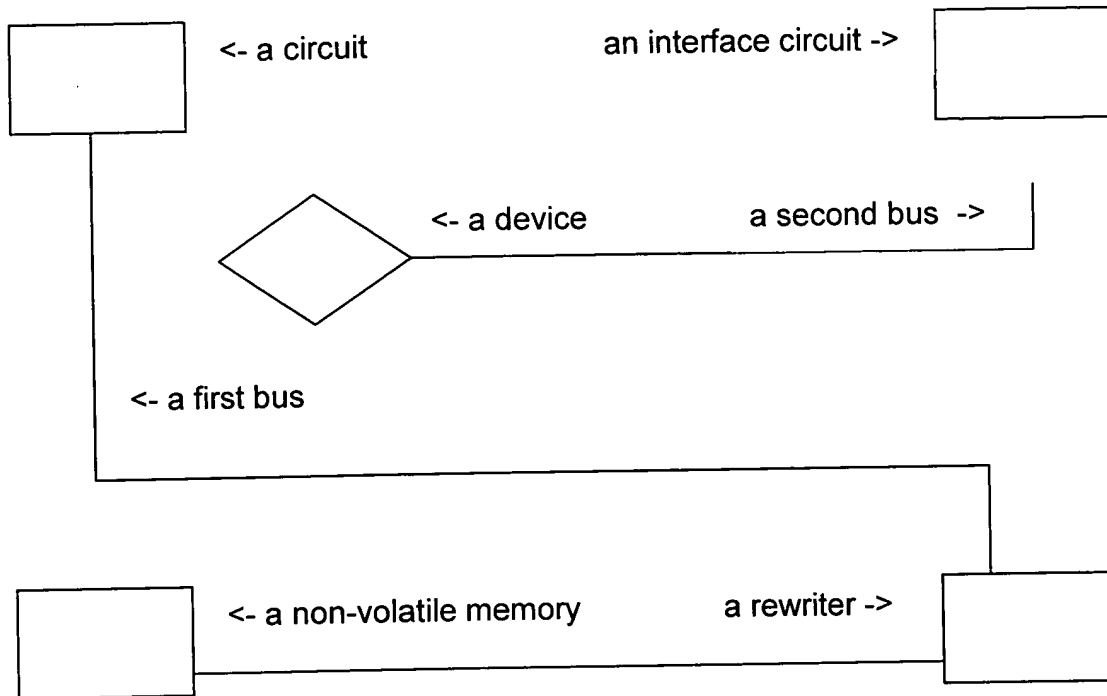
Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-7 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner notes that as amended, claim 1 recites, '...an interface circuit which performs interface processing with a device connected to a second bus ... a rewriter activation section which causes the rewriter to start processing when the second bus is detected to have no connection to any device.' This is indefinite. The last limitation requires the second bus to have no connection to any device, however the interface circuit performs interface processing with a device connected to a second bus. Nothing appears to be recited in the instant claim language which would allow for the disconnection of this device from the second bus to allow the rewriter to begin processing.

The Examiner would further like to illustrate, in the form of the picture shown *infra,* how the Examiner is interpreting the instant claim language in so far as it is clear:

```
[box]        <- a circuit        an interface circuit ->    [box]

        <diamond>   <- a device        a second bus ->

        <- a first bus

[box]  <- a non-volatile memory       a rewriter ->      [box]
```

The Examiner notes that as shown supra, the device is connected to the second bus. No other connections appear to be positively recited, although, the claim does appear to imply connections by reciting, 'data transfers through a first bus ...e.g.', clarification is respectfully requested.

Further the Examiner is also unsure how the rewriter can begin processing as no connection of the second bus to the rewriter appears to be recited; therefore how can a **dis**-connect occur to begin processing?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1-7**, **9**, and **13-14** are rejected under 35 U.S.C. 102(b) as being

anticipated by Bartholomew et al (U.S. 5,978,591) hereinafter referred to as

Bartholomew.

As per independent claim **1**, Bartholomew teach,

- o a circuit which performs data transfer through a first bus, the first bus transferring data conforming to a first interface standard; (Column 9 lines 61-64).

- o an interface circuit which performs interface processing with a device connected to a second bus, the second bus transferring data conforming to a second interface standard; (Column 10 lines 1-4)

- o a non-volatile memory which stores at least one of device information and data transfer control program information; (Column 8 lines 29-34)

- o a rewriter which loads and writes information transferred through the first bus into a rewrite area of the non-volatile memory; and (Column 7 line 61 to Column 8 line 2)

- o a rewriter activation section which causes the rewriter to start processing when the second bus is detected to have no connection to any device (Column 7 lines 36-39 with respect to Figure 8 described in Column 9 line 51 to Column 10 line 8).

- o *The Examiner notes that the first bus, as instantly claimed, is taught by Bartholomew as the bus between the PCMCIA device and the docking station. The second bus, as instantly claimed, is taught by Bartholomew*

as the bus between the computer and the docking station. In the embodiment described in Bartholomew, specifically column 9 line 51 to column 10 line 8, the computer does not have direct PCMCIA connection capabilities. However, the docking station taught by Bartholomew allows the PCMCIA device to be connected to the computer. As taught in column 7 lines 36-39, the embodiment described has a direct PCMCIA connection capability. When the docking station is utilized, the host computer does not see two devices since there is only one connection between the host computer and the docking station (the docking station still being connected to the PCMCIA device) this being equivalent to the direct PCMCIA device to host computer connection. Thus, when the docking station is removed from the host computer but still connected to the PCMCIA device, the rewriting processing can begin as there is no longer a connection to the computer.

As per dependent claim **2**, Bartholomew teach,

- o The data transfer control device as defined in claim 1, wherein the detection of whether or not the second bus is connected to a second device is based on the result of an access to a register of the second device (Column 7 lines 39-44).

As per dependent claim **3**, Bartholomew teach,

- o The data transfer control device as defined in claim 1, wherein the rewriter writes information into the rewrite area by performing data transfer

between the data transfer control device and a first device connected to

the first bus in a mode of loading information to the rewrite area (Column 7

lines 44-48).

As per dependent claim **4**, Bartholomew teach,

- o The data transfer control device as defined in claim 1, wherein data

   transferred from a first device through the first bus is transferred to a

   second device through the second bus, and data transferred from the

   second device through the second bus is transferred to the first device

   through the first bus, in an ordinary operating mode that differs from a

   mode of loading information to the rewrite area (Figure 8 with respect to

   data transfer discussed in the rejection to claim 1 made supra).

As per dependent claim **5**, Bartholomew teach,

- o The data transfer control device as defined in claim 1, wherein the device

   information includes identification information that is specific to an

   electronic instrument in which the data transfer control device is

   embedded (Column 8 lines 29-34).

As per dependent claim **6**, Bartholomew teach,

- o The data transfer control device as defined in claim 1, wherein the non-

   volatile memory has an area in which is stored information for indicating

   whether or not the data transfer control program information has been

   written correctly into the rewrite area (Column 7 lines 44-48). *The*

   Examiner is interpreting the "Code Update" string to be acknowledgement

of whether or not the data transfer control program was written correctly.

This is further taught and shown in Column 7 lines 49-52

As per dependent claim **7**, Bartholomew teach,

- o The data transfer control device as defined in claim 1, wherein: the non-volatile memory has an area in which is stored rewriter processing setting information for setting whether processing by the rewriter is enabled or disabled; and the rewriter processing setting information is set to enabled in an initial state but is set to disabled at the end of processing by the rewriter (Column 6 lines 36-39). *The Examiner notes that at the end of the reprogramming stage, execution is passed to the newly installed application code in the memory. The act of passing execution from the reprogramming stage to the application code, is effectively disabling the reprogrammer and is accordingly disabling the reprogrammer so that execution can then continue.*

As per dependent claim **9**, Bartholomew teach,

- o An electronic instrument comprising: the data transfer control device as defined in claim 1; and a second device connected to the second bus (Column 9 line 51 to Column 10 line 8).

As per independent claim **13**, Bartholomew teach,

- o transferring data through a first bus, the first bus transferring data conforming to a first interface standard; (Column 9 lines 61-64).

o performing interface processing with the second device connected to the second bus, the second bus transferring data conforming to a second interface standard; (Column 10 lines 1-4)

o storing at least one of device information and data transfer control program information in a non-volatile memory; (Column 8 lines 29-34)

o disconnecting the second device from the second bus to start rewriter processing that is activated when the second device is disconnected from the second bus; (Column 7 lines 36-39 with respect to Figure 8 described in Column 9 line 51 to Column 10 line 8).

o loading and writing information transferred through the first bus into a rewrite area by the rewriter processing; and (Column 7 line 61 to Column 8 line 2).

o connecting the second device to the second bus after the writing of the information into the rewrite area (Column 9 lines 28-33).

o *The Examiner notes that the first bus, as instantly claimed, is taught by Bartholomew as the bus between the PCMCIA device and the docking station. The second bus, as instantly claimed, is taught by Bartholomew as the bus between the computer and the docking station. In the embodiment described in Bartholomew, specifically column 9 line 51 to column 10 line 8, the computer does not have direct PCMCIA connection capabilities. However, the docking station taught by Bartholomew allows the PCMCIA device to be connected to the computer. As taught in column*

7 lines 36-39, the embodiment described has a direct PCMCIA connection capability. When the docking station is utilized, the host computer does not see two devices since there is only one connection between the host computer and the docking station (the docking station still being connected to the PCMCIA device) this being equivalent to the direct PCMCIA device to host computer connection. Thus, when the docking station is removed from the host computer but still connected to the PCMCIA device, the rewriting processing can begin as there is no longer a connection to the computer. As taught in Column 9 lines 28-33 Bartholomew further reconnects the device to the host computer. Accordingly, in the event the docking station is utilized, the docking station – still being connected to the PCMCIA device, is reconnected to the host computer.

As per dependent claim **14**, Bartholomew teach,

o   The method of fabricating an electronic instrument as defined in claim 13, wherein the device information includes identification information that is specific to an electronic instrument in which the data transfer control device is embedded (Column 8 lines 29-34).

Response to Arguments

Applicant's arguments filed 21 February 2006 have been carefully and fully considered but are not presuasive.

With respect to applicant's argument located within the first full paragraph of the third page of the remarks (numbered as page 9) which recites:

> *"According to the disclosure of Bartholomew, a circuit which transfers data through the first bus is provided, but Bartholomew does not disclose an interface circuit which executes interface processing between the device which is connected to the second bus"*

The Examiner respectfully disagrees. As shown in the rejection made *supra* and in Bartholomew (figure 8 as well as Column 9 line 51 to Column 10 line 8), a first bus is provided between the PCMCIA device and the docking station. A second bus is proved between the docking station and the computer.

With respect to applicant's arguments located within the first full paragraph of the fourth page of the remarks (numbered as page 10) which recites:

> *"Bartholomew fails to disclose these features."*
> *(Followed by a recitation of claim 1 and claim 13)*

The Examiner respectfully disagrees and refers applicants to the rejection made *supra*.

The Examiner would also like to draw attention to the following comments made within the instant remarks found on the second page (numbered as page 8) which recite:

> *"According to claims 1 and 13, information written into the non-volatile memory is transferred through a first bus. Moreover, the detection of whether the device is connected or disconnected occurs* __at the second bus__ *"(additional emphasis added not present in the remarks)*

The Examiner notes that this is not commensurate in scope with the claim language. The claim language clearly states that processing begins 'when the second

bus is detected to have no connection to any device.' Detection is clearly not occurring

at the second bus but occurring as a result of no connection being present.

The comments noted supra continue on to recite:

"and the detection of whether or not the device is connected to the second bus occurs before information is downloaded through the bus."

The Examiner notes that this as well, is not commensurate in scope with the

claim language. The claim language clearly states 'data transfer through a first bus, the

first bus **transferring** data ......a rewriter which loads and writes information

transferred through the first bus ... when the second bus is detected to have no

connection to any device' (emphasis added). Data is already transferred through the

first bus before the detection of whether or not the device is connected to the second

bus. Thus the detection is happening *after* information is downloaded through the bus.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time
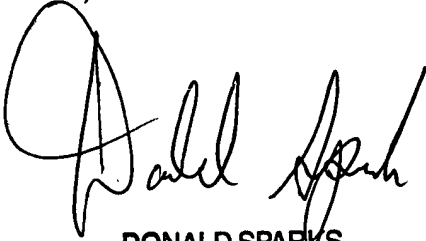
policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAS/mb

DONALD SPARKS
SUPERVISORY PATENT EXAMINER